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PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Oct. 30, 2007 — Date

Beverly Loken

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Adrian J. Drexler	Attorney Docket No.:	501112.01
Patent No.	: US 6,988,218 B2	Serial No.	: 10/074,296
Issue Date	: January 17, 2006	Filed	: February 11, 2002
Title	: SYSTEM AND METHOD FOR POWER SAVING DELAY LOCKED LOOP CONTROL		

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line	Reads	Should Read
Item (54)	"SYSTEM AND METHOD FOR POWER SAVING DELAY LOCKED LOOP CONTROL BY SELECTIVELY LOCKING DELAY INTERVAL"	--SYSTEM AND METHOD FOR POWER SAVING DELAY LOCKED LOOP CONTROL--
Column 1, Lines 1-4	"SYSTEM AND METHOD FOR POWER SAVING DELAY LOCKED LOOP	--SYSTEM AND METHOD FOR POWER SAVING DELAY LOCKED LOOP CONTROL--

	CONTROL BY SELECTIVELY LOCKING DELAY INTERVAL"	
Column 1, Line 10	"delay locked look"	--delay locked loop--
Column 3, Line 32	"recognize that,"	--recognize that--
Column 3, Line 39	"known that, to enable"	--know that to enable--
Column 3, Line 41	"is driven high, that the"	--is driven high, the--
Column 3, Line 55	"will not need not be actively"	--will not need to be actively--
Column 4, Line 25	"and/or disable"	--and/or disabling--
Column 4, Line 35	"device **100**, may be"	--device **100** may be--
Column 4, Lines 54-57	"At that point, if no data is being written to or received by the DRAM device, and there is no need for the DLL **110** to continue switching to fine tune its synchronization with the system clock."	--At that point, if no data is being written to or received by the DRAM device, there is no need for the DLL **110** to continue switching to fine tune its synchronization with the system clock.--
Column 4, Line 63	"FIG. **2** is block diagram"	--FIG. **2** is a block diagram--
Column 5, Line 48	"in at attempt"	--in an attempt--
Column 5, Lines 54-55	"By locking in the delay interval in place once the DRAM device"	--Locking the delay interval in place once the DRAM device--
Column 6, Line 5	"later saves power"	--latter saves power--
Column 8, Line 24	"from the a time the command"	--from a time the command--
Column 8, Line 57	"from the a time the command"	--from a time the command--
Column 9, Line 9	"responsive to command"	--responsive to a command--
Column 9, Line 65	"DRAM devices the computer"	--DRAM devices of the computer--

Column 10, Line 3 "to command" --to a command--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: October 26 2007 By: Edward W. Bulchis

Edward W. Bulchis, Reg. No. 26,847
Customer No. 27,076
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
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Enclosures:
Postcard
Form PTO-1050 (+ copy)

501112.01 req cert correct

UNITED STATES PATENT AND TRADEMARK OFFICE

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DATED : January 17, 2006
INVENTOR(S) : Adrian J. Drexler

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Column 4, Lines 54-57	"At that point, if no data is being written to or received by the DRAM device, and there is no need for the DLL **110** to continue switching to fine tune its synchronization with the system clock."	--At that point, if no data is being written to or received by the DRAM device, there is no need for the DLL **110** to continue switching to fine tune its synchronization with the system clock.--
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MAILING ADDRESS OF SENDER:

Patent No. US 6,988,218 B2

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Seattle, Washington 98101

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FORM PTO-1050 (REV. 3-82)
501112.01 PTO 1050

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